Application Note AN-0008

SDI Router Design Considerations

Introduction

Analogue signals have the problem of continual degradation, whether it be during storage (tape losses), or electrical transfer (noise and waveform distortions). Digital formats were developed to overcome these problems, particularly in multi-pass/multi-generation applications, but have themselves introduced a new set of problems. This application note discusses the digital signal and some of the problems encountered when switching signals through routers.

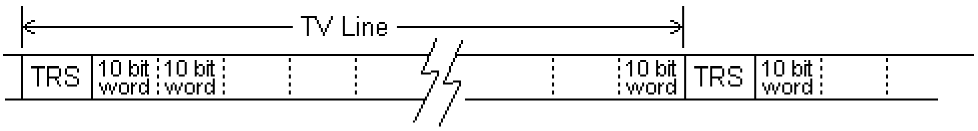
Recent History

The first digital interface standard was parallel video transfer of 8 bits, which was later increased to 10 bits. With a clock speed of 27MHz this was considered fast by the standards of the day. However the practical problems of distributing a 10-bit ECL differential signal soon became apparent and the need was seen for a single wire solution. The only way to get 10 bit data down a single wire is to turn it into serial data.

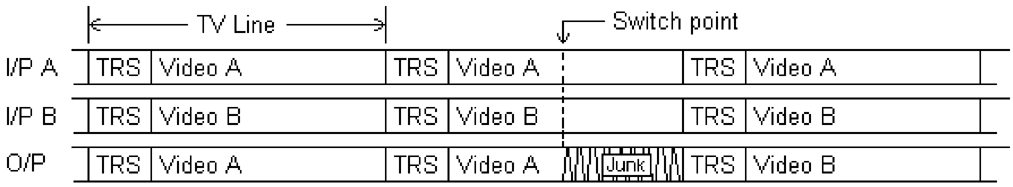
A working serial solution was developed which was one of many possible solutions. This was to place the 10-bit Y, Cr, Y, Cb words into a serialiser and send out the serial sequence at the required 270 million bits per second (270Mb/S). To help de-serialise the data at the receiving end, a special sequence called the TRS or Timing Reference Signal was included, and this is the equivalent of the sync in analogue video signals.

The TRS sequence is a 10 bit word of all one's (high's) followed by two words of all zero's (lows), written in hexadecimal format as 0x3ff + 0x000 + 0x000. A fourth word contains extra horizontal and vertical timing information. Serial video de-serialiser IC's have a special circuit to detect TRS words and then reset their serial-to-parallel converters. There are actually two TRS words per TV line, one at the start of active video (SAV TRS) and one at the end of active video (EAV TRS). The period between EAV and SAV contains embedded audio and other ancillary data.

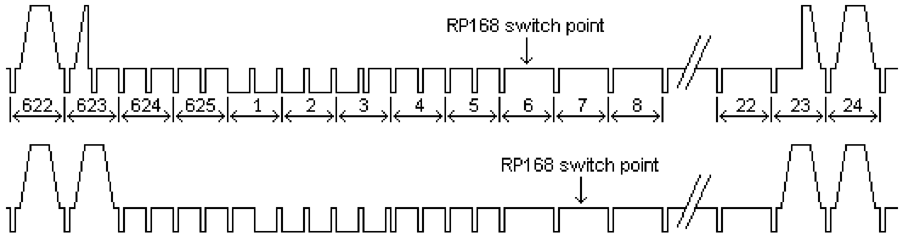
When the SDI signal is moved around the studio through routers and other distribution equipment, it should only be thought of as a digital data stream rather than in terms of video pictures. The data stream length is either 1728 words of 10 bits each (625 line systems) or 1716 words (525 line systems)..



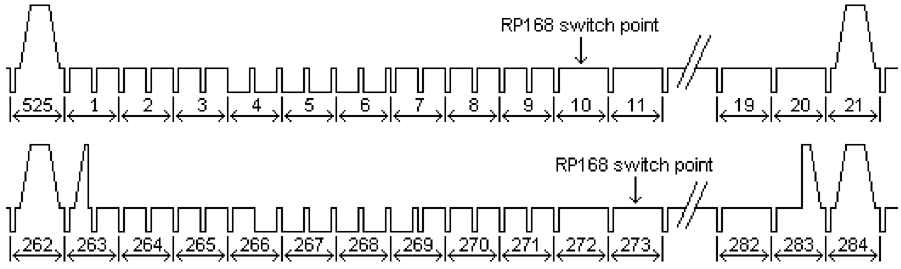
When a router switches this data stream, some corruption of the data is inevitable. This is because each bit of a 10-bit word is only 3ns wide and cable length inequalities introduce timing skews of 5ns per meter. Assuming a 1/4 bit timing error is acceptable, then this equates to a maximum cable length difference of 0.15m, before errors occur. In practice the data from the switch point to the next TRS word can be assumed to be corrupted and should be ignored.



SMPTE recognised this problem and introduced a recommended practice, RP-168, to encourage equipment manufacturers to only switch the serial data stream in the centre of line 6 in 625 line systems and line 10 in 525 line systems.

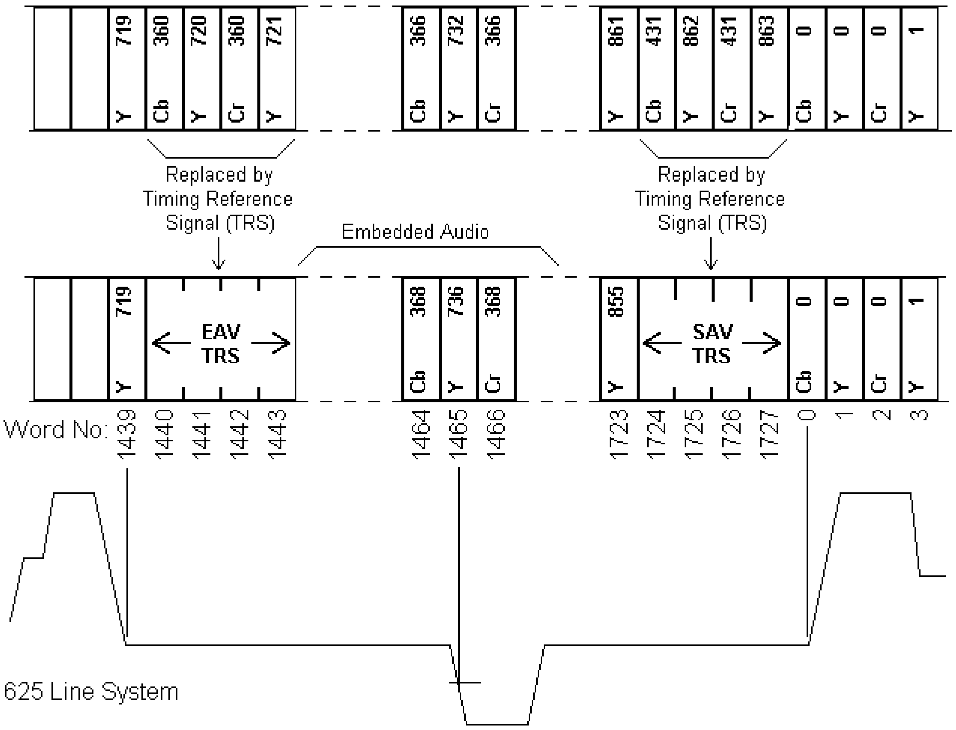


625 Line System



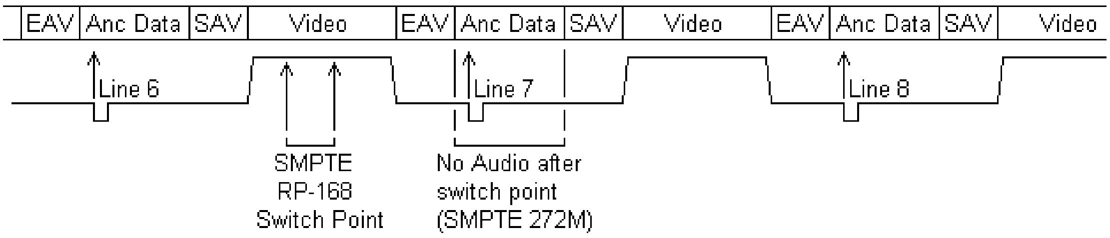
525 Line System

This allows equipment downstream of the router the maximum number of lines before active picture to recover from the switch. Looking in a bit more detail at the video structure:



625 Line System

The block after EAV and up to SAV is an ancillary data and the embedded audio is contained immediately after the EAV TRS sequence. Applying the RP-168 switch point for 625 line systems gives the following sequence.



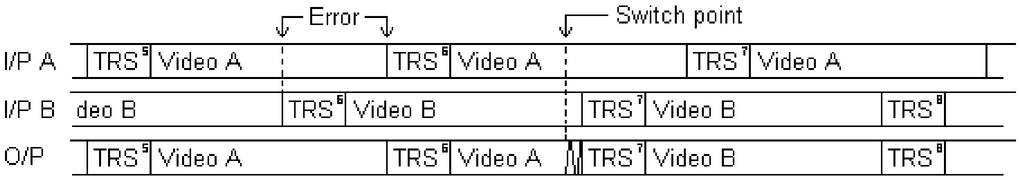
Note the comment about no audio after the switch point, this was a later amendments to SMPTE 272M to prevent embedded audio 'clicks' during video switching.

Quartz routers comply with RP-168 and derive the switch point from an analog reference input. The switch actually occurs at a point 30us (+/-5us) after the falling edge of the line sync pulse on the lines shown above.

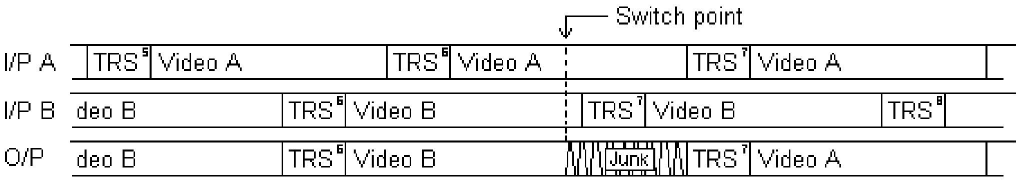
Horizontal Timing Problems

From the ideas discussed so far, it is possible to derive what might be the maximum allowable timing error before problems occur. It should be noted here that most routers can cope with any amount of timing error and it is the downstream equipment (equipment after the router) that shows the problem as a picture or other disturbance.

Consider the two mis-timed signals (less than +/-23uS error to reference) shown below:

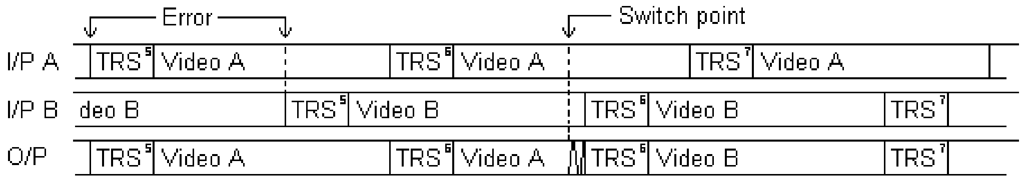


Note the line numbers indicated in the TRS words. Switching from i/p A to i/p B causes the o/p to have two TRS words close together. If this were fed to a SDI-to-RGB convertor to drive a picture monitor, the analogue waveform would have two line sync pulses very close together. Switching from i/p B back to i/p A will give a sequence with a larger than normal gap between TRS words.

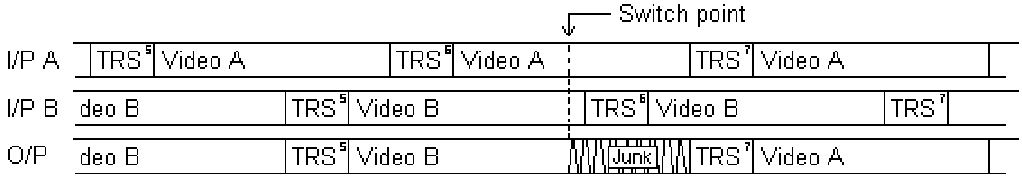


This difference when switching from i/p A to i/p B and then back again can be used as a simple diagnosis for timing errors i.e. if a disturbance is worse switching one way then suspect mistimed router inputs. Why downstream equipment responds differently, depending on the direction of the switch, is normally related to phase locked loop re-lock times. The timing figure of 23uS was chosen as it can take the router video TRS to within 2uS and 6uS of the RP-168 switch point.

Now consider the very badly timed signals (greater than +/-35uS error to reference) shown below:



Note the line numbers indicated in the TRS words. Switching from i/p A to i/p B in the centre of line 6 causes the o/p to have two line 6 TRS words close together. This equates to a frame with 626 or 526 lines. If this were fed to a SDI-to-RGB converter to drive a picture monitor, the analogue waveform would have the wrong number of lines and a TV monitor would almost certainly show a small vertical bounce. Switching from i/p B back to i/p A will give a sequence with a missing line 6.



From this we can say that all timing errors should be minimised, and the timing error of any router input should certainly be no greater than ±23uS to the reference. We can also test real world equipment by applying timing errors to a router and tests at Quartz indicate that there are big differences between manufacturers. In some cases third party equipment will cope well with the video signal but introduce errors to the embedded audio.

For video performance there is a big performance difference between Component (RGB/YUV) and Composite (PAL/NTSC) converters. Tests on a range of monitoring quality composite D-to-A convertors (PAL/NTSC) and picture monitors show that the worst-case timing error should not exceed the values below.

Manufacturer	**Encoder**	**Timing Difference**	**Cable Equivalent**
Axon	SA-23	25nS	5.00m
BAL	SAC012B	10nS	2.00m
Metawave	MW-97	1.5ns	0.30m
Sony	BKPF-L613C	20ns	4.00m
Vistek	V1627	0.8nS	0.16m

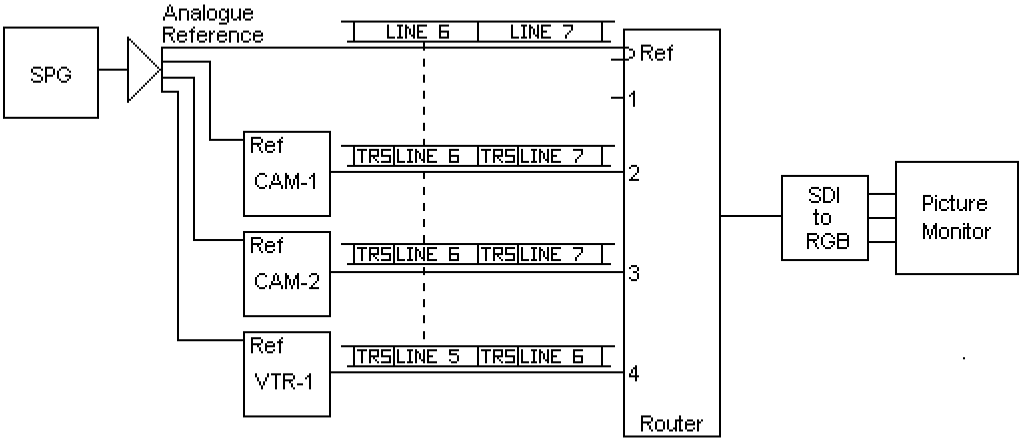
If a system uses monitoring quality PAL encoders then switching disturbances will be seen unless the router inputs are timed to within the above figures (almost impossible) or a line/frame synchroniser is used on the router output. If neither of these options can be used then consider using broadcast quality PAL encoders with a separate sync input or component converters.

Tests on a range of Component D-to-A converters (RGB/YUV) and picture monitors show that the worst-case timing error should not exceed ±2uS (microseconds) with respect to the reference. This will cause a maximum jump in sync timing of 4uS when switching between the earliest and latest signals.

In all cases the input video timing with respect to the reference is less critical. As a system design rule there should be no router input signals outside a ±23uS window with respect to the reference.

Vertical Timing Problems

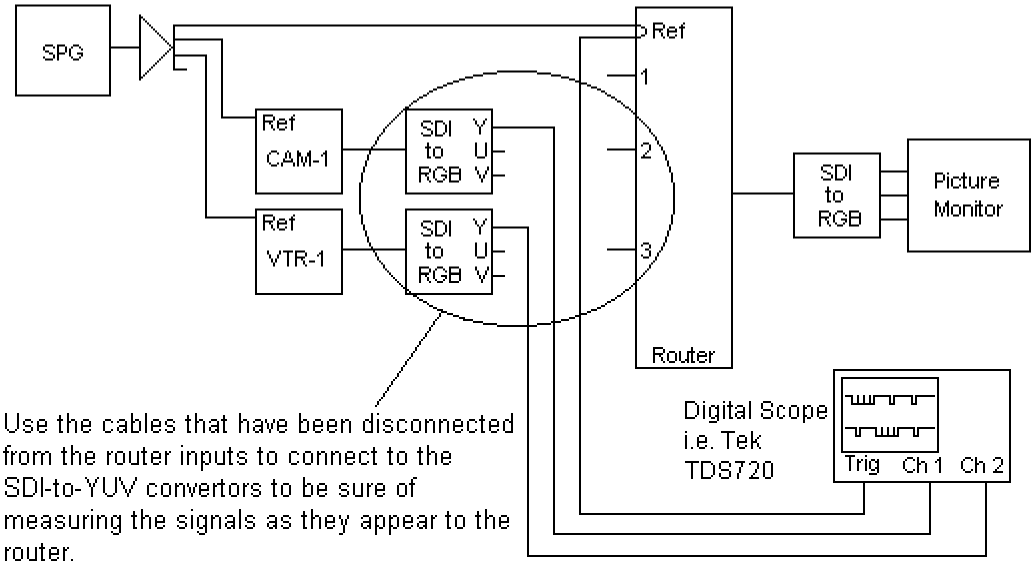
In a real studio set-up it is not minor timing inequalities that cause most problems. A lot of digital video equipment generates internal clock signals from an external analogue reference. From these clock signals the equipment can generate its SDI output but often with a line delay between the reference input and the SDI output. This is shown for the VTRs in the diagram.



The Sync Pulse Generator (SPG) is used as the master reference for all equipment. The router will derive its SMPTE RP-168 switch point from this reference causing the router to switch in the centre of line 6. The camera CAM-1 and VTR-1 are generating video that is locked and co-incident with the SPG timing, and so switching between CAM-1 and VTR-1 will give a clean switch. VTR-2 is also locked to the SPG but its o/p timing is one line delayed, so switching between CAM-1 and VTR-2 will cause a one-line jump on the monitor. If a more complex downstream converter were used, such as SDI-to PAL, then a disturbance may be seen lasting a whole field.

There are two solutions to this problem. The VTR may have an adjustment to allow its output timing to be altered. If there is sufficient adjustment range to get co-incident timing with the reference, then this method should be used. If there is not sufficient adjustment then an SPG with individually adjustable reference outputs will be required. Use these adjustable SPG outputs to generate a new reference signal that is one line early, and use this to lock up the VTRs. The VTR output timing shift will then be compensated by the early reference input.

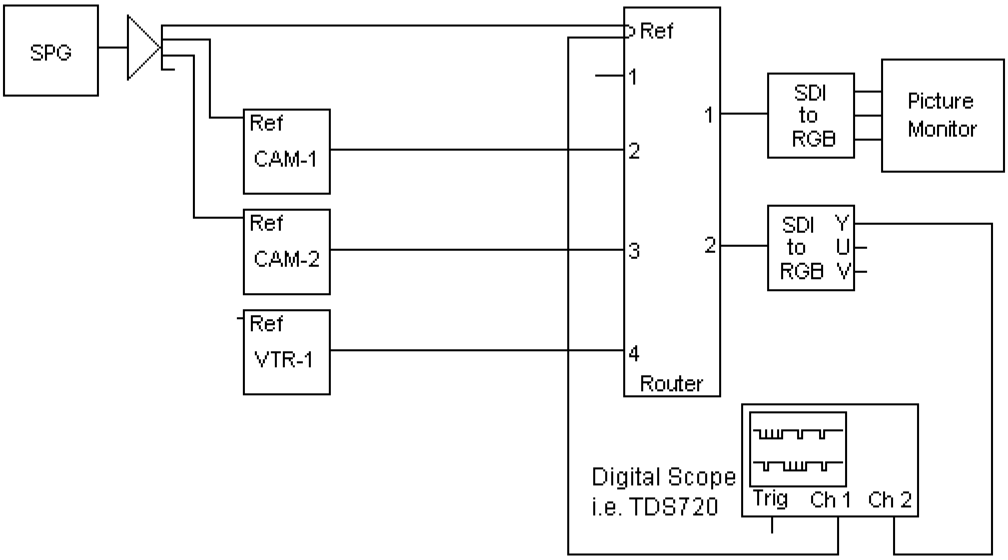
If it is not clear exactly what signal timing is being generated by various pieces of equipment, then use the following method to analyse the problem.



Note that SDI-to-YUV or RGB converters are used as these give the most direct view of the SDI signal. Do not use SDI-to-PAL converters, as these will often have significant internal time delays. Make sure that the converters are identical so that they both have the same delay and make sure they do NOT contain a front end line or frame synchroniser. A lot of oscilloscopes have a TV trigger but this usually only operates at line or field rate. To correctly view the signals the scope should ideally be triggered at frame/picture rate.

It is normally easier to set the scope up by connecting the reference signal to channel 1 and trigger the scope so that the vertical sync lines up with a screen graticule. Then move the reference signal to the trigger input, remembering to alter the trigger menu options, and view the first SDI converted signal on channel 1. The vertical sync should again line up with the same screen graticule, confirming that channel 1 has the same timing as the reference signal. Channel 2 can then be connected to allow direct comparisons of the SDI converted waveforms. The time base will have to be used in two modes. First use a slow time base to compare the vertical or frame sync area of the waveform, ensuring that both SDI signals have co-incident frame and line timing, then use a faster time base to compare the line sync edges. Channel 2 can now be replaced with any other SDI signals to check as many router inputs as required.

An alternative method is to look at the signals after the router.



In this example the router is used to select a source (CAM-1) and its timing is compared with the reference. Use an on-screen time cursor, if your scope supports this function, to mark the vertical sync edge. Now use the router to select another source (VTR-1) and again compare the timing to the reference. Use the scopes second time cursor to measure the time between the sources sync edges.

Serial Transmission And Data Recovery

As stated earlier, a working SDI solution was developed which was one of many possible solutions, which was to simply place the 10 bit Y, Cr, Y, Cb words into a serialiser and send out the serial sequence at 270Mb/S. No clock signal was incorporated with the data, to keep the bit rate to a minimum, but this makes signal recovery difficult. Although no clock signal is sent with the data, the clock rate can be ‘worked out’ by measuring the minimum time between rising and falling edges of the data, and this is one of the functions of a Phase Locked Loop or PLL.

The problem of data and clock recovery is compounded by the fact that a black picture would cause long streams of 0’s (or 1’s for white), so a randomiser, or scrambler, was used to scramble the signal. The scrambling is a mathematical function that can be reversed at the receiving end.

However, a problem exists with the scrambler because certain patterns of 1’s and 0’s cancel out the effect of the scrambler and cause long streams of 1’s and 0’s. These patterns are known as pathological test signals and it is important to test equipment for its ability to pass pathological test signals. Pathological type signals are often generated by paint box systems when areas are colour filled.

The other problem with serial 270Mb/s signal transmission is cable loss, which is approximately 0.1dB/meter (measured at 270Mhz). This means that at the end of 300m of cable the high frequency losses are greater that 30dB. To recover this signal an adaptive cable equaliser is used. This is an automatically adjusted, frequency dependent amplifier that compensates for the cable loss. This ‘recovered’ signal is not perfect and suffers from wave shape distortions. A fast comparator can be used to slice the signal to give a cleaner waveform, but the wave form still suffers from some mark/space ratio degradation, meaning that some bits will be wider (or narrower) than they should be. A further processing stage can be applied by a phase locked loop that synthesises a clock signal of at least twice the data rate, and then uses this clock to re-clock the data. The problem with PLLs is that they suffer from jitter on the synthesised clock, which is imposed back onto the re-clocked data.

To route or distribute a serial video signal there are 3 possible solutions, pass the signal in an analogue form, pass the cable equalised signal, or pass a cable equalised and re-clocked signal. Passing an analogue signal will work but as the signal needs to be recovered at some point, the total signal path must not exceed 300m. Passing an *equalised only* signal will also work but the signal will have gained higher frequency components due to mark/space distortion. These suffer greater losses down the cable, which in turn reduces the maximum length of cable that can be used. This leaves us with the option of ‘equalise and re-clock’. This is the method currently used by most routing and distribution equipment.

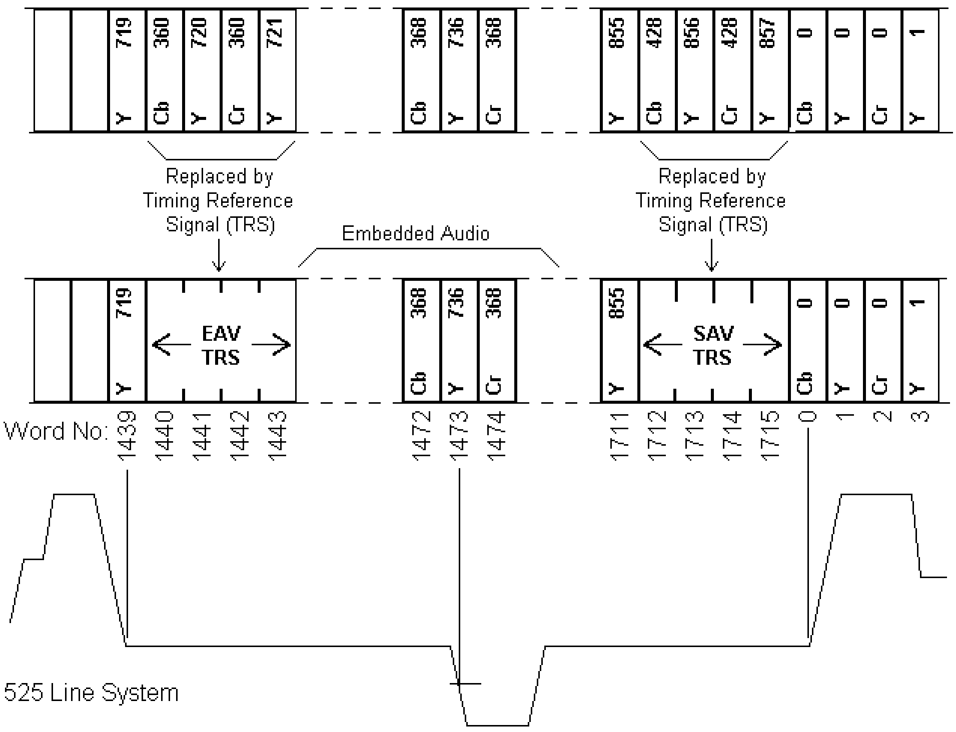
The main difficulty with any re-clock method is PLL jitter. PLL adjustment also used to be a problem but has now been eliminated by PLLs that auto adjust. As all PLL designs suffer from some jitter, each reclocking stage will introduce more jitter into the signal. After multiple passes through reclocking stages, perhaps 20, the jitter will be so bad that the signal is unrecoverable. It should be pointed out here that any equipment that converts the signal back to the parallel domain will usually stop this jitter build-up by re-serialising from a clean, crystal oscillator derived, 27MHz clock. To minimise total jitter in a system, each piece of equipment should minimise it own jitter contribution. This is largely controlled by the internal design of the serial receiver chip set and the circuit board layout.

Equipment tests

When buying equipment it is important to verify that the serial digital I/O works correctly. Equipment should be checked for its ability to pass pathological test patterns. This check should also be made with long input cables to verify the cable equalisation, and short cables to test for input return loss problems. Input and output return loss can be measured but this requires very specialised equipment. Output amplitudes need to be checked as a low or high level can reduce the maximum cable run to the next stage. Lastly, jitter performance should be checked with various cable lengths. This also requires specialised test equipment.

Appendix A: 525 Data Structure

The 525-line horizontal data structure is shown below.



Appendix B: Relevant Standards

SMPTE RP-168	Switching Points for Serial Digital and Analog Interfaces
SMPTE 125M	Component Video Signal 4:2:2 Bit-Parallel Digital Interface
SMPTE 259M	10-Bit 4:2:2 Component and 4fsc Composite Digital Signals
SMPTE 272M	Formatting AES/EBU Audio into Digital Video Ancillary Data Space
EBU T3267	EBU Interfaces for 625 Line Digital Video Signals at 4:2:2 Levels